

In the Claims

1. **(As Filed)** In a processing system having an unprotected pipeline, an apparatus comprising:

5 a first logic gate for providing a first signal when a halt signal and a non-interruptible code signal occur together, and

 a memory unit for storing the first signal, the first signal indicating a non-returnable interruption of the
10 executing procedure.

2. **(As Filed)** The apparatus as recited in claim 1 wherein the first signal is transferred to a read bus.

15 3. **(As Filed)** The apparatus as recited in claim 1 wherein the memory unit is a memory-mapped register location.

20 4. **(As Filed)** The apparatus as recited in claim 1 wherein the first logic gate is a logic AND gate.

Please amend Claim 5 as follows.

25 5. **(Currently Amended)** The apparatus as recited in claim 1 further comprising:

 a second logic gate, and

 a memory unit, the second logic gate providing a halt signal when a trigger signal is applied to a first input

terminal and the contents of the memory unit are applied to a second input terminal.

6. **(As Filed)** A method for transferring a halt
5 signal when a halt signal occurs during a non-interruptible
portion of the executing code of a processor having a non-
protected pipeline, the method comprising:
determining when a halt signal occurs during a non-
interruptible portion of the executing code, and
10 storing a non-returnable bit in a memory location
accessible to testing device.

7. **(As Filed)** The method as recited in claim 6
wherein, when the control signal is applied to the memory
15 location, applying the non-returnable bit to a read bus.

8. **(As Filed)** The method as recited in claim 7
wherein the memory unit is a memory-mapped register.

20 9. **(As Filed)** A data processing unit comprising:
a processor, the processor including:
a non-protected pipeline,
the processor executing interruptible code and
non-interruptible code;
25 an event signal generating unit, the event signal
generating unit generating an event signal in response to a
halt condition;

a logic unit responsive to the halt condition and
a control signal for generating a halt trigger signal
during a non-interruptible code portion; and

a storage unit for storing a non-returnable bit
5 in response to the trigger halt signal.

10. **(As Filed)** The processing unit as recited in
claim 9 wherein the storage unit is a memory-mapped
register, the memory mapped register responsive to a
10 control signal for transferring the non-returnable bit
outside of the processor.

Please amend Claim 11 as follows.

15 11. **(Currently Amended)** The processing unit as
recited in claim 10 further including a storage unit, the
storage unit storing an first signal when the processing
unit is executing non-interruptible code, the ~~first~~ first
signal stored in the storage unit providing the control
20 signal.